the width of irradiation pattern can be continuously controlled according to changes in ion acceleration energy, and the vertical distribution of implanted ions shows an excellent uniformity.

(2) A second conductivity-type region is formed by changing only the acceleration energy after a first conductivity-type region is formed on a silicon substrate using a shield mask made of a photoresist having stripes of openings with a predetermined aperture width. Then although the vertical distribution of ions becomes relatively less uniform, a super junction can be formed using only the common ion implantation equipment and PEP without conducting ion beam sweep.

(3) If a first and second conductivity-type regions are formed by ion irradiation onto an intrinsic silicon substrate by the use of a shield mask made of a photoresist with striped shape openings of a specific width and another shield mask made of a photoresist in the reversed relation to the above photoresist, a uniform super junction is formed in the vertical direction because the lateral broadenings of ions compensate each other due to scattering.

(4) If a collimated neutron beam is irradiated onto a P^+ silicon ingot, a uniform super junction is formed there, because the transmission coefficient of neutron beam is high enough to precisely transmute the irradiated region into an N^+ region with less broadening. If the neutron beam is irradiated in parallel with the growth axis of the silicon ingot and silicon wafers are sliced out in the direction vertical to the growth axis as is the case with common silicon wafers, many silicon substrates each having a precision super junction over its surface can be produced at a time.

Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details and representative embodiments shown and described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.

What is claimed is:

1. A semiconductor device manufacturing method of forming a second conductivity-type region by irradiating impurity ions onto a first conductivity-type semiconductor substrate;

wherein the impurity ion irradiated region is restricted by a shield mask intercepting said impurity ions and the impurity ion acceleration energy is controlled to provide a uniform impurity distribution in the direction of irradiation in said second conductivity-type region.

2. A semiconductor device manufacturing method of forming at least one of a first and second conductivity-type regions in a semiconductor substrate by selectively irradiating impurity ions onto said semiconductor substrate;

wherein the impurity distributions in said first and second conductivity-type regions are uniform in the direction of irradiation, and the impurity ion acceleration energy and the area of each region irradiated by said impurity ions are controlled so that the cross-sectional shape and cross-section area of said first and second conductivity-type regions on planes perpendicular to the direction of irradiation may be uniform in the direction of irradiation.

3. The semiconductor device manufacturing method according to claim 2, wherein the control of the area of said irradiated region comprises the steps of forming an ion beam made of impurity ions and sweeping the ion beam in the vertical and horizontal directions on the irradiated region, and the acceleration energy and the area of the irradiated region are controlled by changing the area of said irradiated region according to changes in said acceleration energy.

4. The semiconductor device manufacturing method according to claim 3, wherein said impurity ion beam is electrically swept on the irradiated region.

5. The semiconductor device manufacturing method according to claim 3, wherein said impurity ion beam is magnetically swept on the irradiated region.

6. The semiconductor device manufacturing method according to claim 3, wherein said impurity ion beam is swept on the irradiated region by moving the semiconductor substrate.

7. The semiconductor device manufacturing method according to claim 3, wherein the acceleration energy and the area of the irradiated region are controlled by decreasing the area of the irradiated region according to increase in the acceleration energy.

8. The semiconductor device manufacturing method according to claim 3, wherein the acceleration energy and the area of the irradiated region are controlled by increasing the area of the irradiated region according to decrease in the acceleration energy.

9. The semiconductor device manufacturing method according to claim 2, wherein the area of the irradiated region is restricted by a shield mask intercepting said impurity ions, and the acceleration energy and the area of the irradiated region are controlled by changing the area of each opening of said shield mask intercepting impurity ions according to changes in the acceleration energy.

10. The semiconductor device manufacturing method according to claim 9, wherein the acceleration energy and the area of the irradiated region are controlled by decreasing the area of each opening of said shield mask intercepting impurity ions according to increase in the acceleration energy.

11. The semiconductor device manufacturing method according to claim 9, wherein the acceleration energy and the area of the irradiated region are controlled by increasing the area of each opening of said shield mask intercepting impurity ions according to decrease in the acceleration energy.

12. A semiconductor device manufacturing method of forming a first conductivity-type region and a second conductivity-type region on a semiconductor substrate by irradiating impurity ions onto said semiconductor substrate;

wherein the regions irradiated by impurity ions are restricted by impurity ion intercepting shield masks which are in an inverted imaging relation to each other so that the cross-sectional shape and the cross-section area of the first and second conductivity-type regions on planes perpendicular to the direction of irradiation may be uniform along the direction of irradiation, and the impurity ion acceleration energy is controlled to make the impurity ion distributions in the first and second conductivity-type regions uniform along the direction of irradiation.

13. The semiconductor device manufacturing method according to claim 12, wherein said impurity ion intercepting shield masks which are in an inverted imaging relation to each other are formed by printing the same mask patterns on the semiconductor substrate by the use of a positive resist and a negative resist.

14. A semiconductor device manufacturing method of forming an N^+ region by irradiating a neutron beam onto a semiconductor ingot having a P^+ region;

wherein the incident direction of said neutron beam is collimated to make the cross-sectional shape and the cross-section area of said N^+ region on planes perpendicular to the direction of irradiation uniform along the direction of irradiation, and the impurity distribution in said N^+ region is controlled to be uniform along the direction of irradiation.

15. The semiconductor device manufacturing method according to claim 14, wherein the semiconductor having the P^+ region is an P^+ type semiconductor ingot and the incident direction of said neutron beam is parallel to the growth axis of said P^+ type semiconductor ingot.

16. The semiconductor device manufacturing method according to claim 14, wherein said semiconductor ingot is made of silicon.

17. The semiconductor device manufacturing method according to claim 14, wherein said semiconductor ingot is made of germanium.

18. The semiconductor device manufacturing method according to claim 14, wherein said semiconductor ingot is made of silicon carbide.

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